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Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Fusen Chen, et al. §

Serial No.: 08/856,116 §

Filed: May 14, 1997 §

For: Reliability Barrier Integration §
For CU Application §

Group Art Unit: 2814

Examiner: G. Peralta

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Assistant Commissioner of Patents
Washington, D.C. 20231

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Date	Signature

Dear Sir:

APPEAL BRIEF

Applicants submit this Appeal Brief to the Board of Patent Appeals and Interferences on appeal from the decision of the Examiner of Group Art Unit 2814 dated October 10, 2001, finally rejecting claims 15-18, 21, and 23. Please charge the fee of \$320.00 for filing this brief, and any additional fees to make this submission timely, to Deposit Account No. 20-0782/APPM/1931/KMT. A duplicate copy of this letter is enclosed. Three copies of this brief are submitted for use by the Board.

Real Party in Interest

The present application has been assigned to Applied Materials, Inc., 3050 Bowers Avenue, Santa Clara, California 95054.

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Related Appeals and Interferences

Appellant asserts that no other appeals or interferences are known to the appellant, the appellant's legal representative, or assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

Status of Claims

Claims 15-18, 21, and 23 are pending in the application. Claims 1-20 were originally presented in the application. Claims 21-24 were added during prosecution, and claims 1-14, 19-20, 22, and 24 were canceled without prejudice by the Applicants during prosecution. Claim 19 was restricted and canceled without prejudice by Applicants during prosecution. Claims 15-18, 21, and 23 stand rejected in view of a combination of references as discussed below. The rejection of claims 15-18, 21, and 23 is appealed. The pending claims are shown in the attached Appendix. No claims have been allowed.

Status of Amendments

The claims in the Appendix include all amendments presented by Applicants, which amendments were entered by the Examiner prior to filing of this Appeal Brief.

Summary of the Invention

The claimed invention generally provides a method for filling a feature with copper. In one embodiment, the method comprises first forming a reliable barrier layer in the feature to prevent diffusion of the copper into the dielectric layer through which the feature is formed. The method for filling a feature formed in a dielectric comprises forming a generally conformal first barrier layer 16 over a patterned dielectric 12, removing the portion of the first barrier layer 16 formed on the bottom 22 of the feature 20, depositing a second barrier 24 comprising a material selected from a group consisting of Ta, TaN, TaSiN, TiSiN, and combinations thereof, and then filling the feature 20 with copper. (See page 6, lines 5-22; see also Example 1, page 12, line 22, to

page 13, line 7, and Figures 2-6) In another embodiment, the method comprises depositing a first barrier layer 16 over a blanket dielectric layer 12, forming a feature 20 through both the barrier layer 16 and the dielectric layer 12, depositing a second barrier layer 30 in the feature 20, removing the barrier layer 30 from the bottom of the feature 20, and selectively depositing a metal layer in the feature 20. (See page 6, line 23, to page 7, line 11; *see also* Example 2, page 13, lines 8-16, and Figures 7-12).

Issues Presented

1. Whether the Examiner erred in rejecting claims 15-18, 21, and 23 under 35 U.S.C. § 103(a) as being unpatentable over *Taguchi et al.* in view of *Zhao et al.* and *Silwa et al.*

Grouping of Claims

Pending claims 15-18, 21, and 23 do stand or fall together for all arguments presented by Applicant. Applicant's argument relates to claims 15-18, 21 and 23, and claim 15 is representative of the claims.

ARGUMENT

I. THE EXAMINER ERRED IN REJECTING CLAIMS 15-18, 21 AND 23 UNDER 35 U.S.C. § 103(a) BECAUSE THE CITED REFERENCES DO NOT TEACH, SHOW, OR SUGGEST DEPOSITING A FIRST BARRIER LAYER OVER A BLANKET DIELECTRIC LAYER, FORMING A FEATURE THROUGH THE FIRST BARRIER LAYER AND THE DIELECTRIC LAYER TO EXPOSE AN UNDERLAYER, DEPOSITING A SECOND BARRIER LAYER ON THE BOTTOM AND SIDEWALLS OF THE FEATURE, REMOVING THE SECOND BARRIER LAYER FORMED AT THE BOTTOM OF THE FEATURE, AND SELECTIVELY DEPOSITING A METAL LAYER ON THE UNDERLAYER EXPOSED IN THE FEATURE.

Claims 15-18 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Taguchi et al.* in view of *Zhao et al.* and *Silwa et al.*, on grounds that

the combination of references shows each feature of the claimed invention. Applicants respectfully traverse this rejection on grounds that the claims include the novel combination of depositing a barrier layer that is removed to expose an underlayer within a feature, and selectively depositing a metal layer on the underlayer to fill the feature as described in the specification and Figures 7-11.

To determine patentability under 35 U.S.C. § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved, and the obviousness or non-obviousness of the subject matter is determined against this background. *Graham v. John Deere*, 383 U.S. 1 (1966). Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). To establish prima facie obviousness of a claimed invention, all the claimed limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Taguchi et al. discloses deposition of a first silicon nitride (SiN) layer 21 over a PSG layer 20, etching a contact hole 20a to a silicide layer 17a, depositing a second SiN layer 22 on the silicon nitride layer 21 and the silicide layer 17a, etching the SiN layer 22 so that only the walls of the contact hole 20a are covered with the second silicon nitride layer 22a, depositing a conformal titanium barrier layer on the second silicon nitride layer 22a and the silicide layer 17a in order to provide an improved wetting surface for aluminum fill of a hole. (See, col. 7, lines 32-63, and Figures 6-11) *Taguchi et al.* teaches the formation of a barrier layer on the bottom of a hole prior to deposition of aluminum and teaches that layers are non-selectively deposited. *Taguchi et al.* does not disclose selectively depositing a metal layer on the underlayer exposed in the feature.

Zhao et al. discloses depositing a interlayer dielectric (ILD) layer 12 over a titanium nitride (TiN) barrier layer 13 disposed on a metal 11, etching the ILD layer 12 to

expose the TiN barrier layer 13 (or optionally etching the ILD layer 12 and the TiN barrier layer 13 to expose the metal 11) by a via 15, depositing a dielectric layer 16 over the ILD layer 12 and the exposed portion of TiN layer 12 (or optionally, metal 11) within the via 15, etching the dielectric layer 16 to remove the dielectric layer 16 from the surface of the ILD layer 12 and the bottom of the via 15 to retain dielectric layer 16 on the sidewalls 17, and depositing an activation layer 21 (or optionally 27) on the exposed bottom of the via 15 prior to depositing a plug 23. (See, col. 5 line 47, to col. 7, line 35, and Figures 2-6, see also col. 9 line 11, to col. 10, line 28, and Figures 7-13. *Zhao et al.* does not disclose depositing a first barrier layer over a blanket dielectric layer and forming a feature through the first barrier layer and the dielectric layer to expose an underlayer.

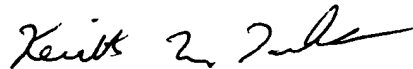
Sliwa et al. discloses the use of sidewall spacers of a conductive material on an aluminum interconnect to improve oxide planarization and inhibit whisker formation and voiding due to electromigration in aluminum interconnect formation. *Sliwa et al.*, does not disclose depositing a first barrier layer over a blanket dielectric layer, forming a feature through the first barrier layer and the dielectric layer to expose an underlayer, depositing a second barrier layer on the bottom and sidewalls of the feature, removing the second barrier layer formed at the bottom of the feature, and selectively depositing a metal layer on the underlayer exposed in the feature.

Taguchi et al., *Zhao et al.*, and *Sliwa et al.*, alone or in combination, do not teach, show, or suggest depositing a first barrier layer over a blanket dielectric layer, forming a feature through the first barrier layer and the dielectric layer to expose an underlayer, depositing a second barrier layer on the bottom and sidewalls of the feature, removing the second barrier layer formed at the bottom of the feature, and selectively depositing a metal layer on the underlayer exposed in the feature, as recited in claim 15, and claims dependent thereon. There is no suggestion or motivation to combine *Taguchi et al.*'s conformal titanium barrier layer in order to provide an improved wetting surface for aluminum fill of an opening with *Zhao et al.*'s deposition of an activation layer 21 on the exposed bottom of the via 15 prior to deposit a plug 23. Reversal of the rejection of claims 15-18, 21, and 23 is respectfully requested.

Conclusion

In conclusion, the references do not teach, show, or suggest depositing a first barrier layer over a blanket dielectric layer, forming a feature through the first barrier layer and the dielectric layer to expose an underlayer, depositing a second barrier layer on the bottom and sidewalls of the feature, removing the second barrier layer formed at the bottom of the feature, and selectively depositing a metal layer on the underlayer exposed in the feature. Thus, Applicants respectfully request withdrawal of the rejection of claims 15-18, 21, and 23.

Respectfully submitted,



Keith M. Tackett
Reg. No. 32,008
Attorney for Applicant
MOSER, PATTERSON, & SHERIDAN, L.L.P.
3040 Post Oak Boulevard, Suite 1500
Houston, Texas 77056
(713) 623-4844

APPENDIX

15. A method of filling a feature in a dielectric layer, comprising:
- a) depositing a first barrier layer over a blanket dielectric layer;
 - b) forming a feature through the first barrier layer and the dielectric layer to expose an underlayer;
 - c) depositing a second barrier layer on a bottom and sidewalls in the feature;
 - d) removing the second barrier layer formed at the bottom of the feature;
 - and
 - e) selectively depositing a metal layer on the underlayer exposed in the feature.
16. The method of claim 15, wherein the first barrier layer and the second barrier layer comprise Si_xN_y .
17. The method of claim 16, wherein the first barrier layer and the second barrier layer are formed using chemical vapor deposition techniques.
18. The method of claim 17, wherein the second barrier layer is removed from the bottom of the feature by sputter etching techniques.
21. The method of claim 15, wherein the metal layer comprises copper.
23. The method of claim 15, wherein the metal layer is deposited using electroplating techniques.